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Sir:

Attached please find the application papers of Ikuo ASO, Sakae WATANABE, Isao WADA, Kazumasa AZUMA, covering new and useful improvements in LINE SWITCHING SYSTEM AND LINE SWITCHING UNIT OF DYNAMIC BAND VARIATION UNIT, comprising:

Specification, Seven (7) Claims and Abstract of the Disclosure (25 pages)

English language, Combined Declaration and Power of Attorney (2 pages)

Seven (7) Sheets of Drawings Showing Figures 1-7

Letter Claiming Right of Priority and Certified Copy of Japanese Patent Application No. 10-128973

Assignment and Recording of Assignment Letter

U.S. Government Filing Fee of $760.00

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Please charge any shortages in the fees or credit any overpayments thereof the deposit account of Antonelli, Terry, Stout & Kraus, LLP Account No. 01-2135 (648.37184X00).

Respectfully submitted,

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JND/nac
Attachments

LINE SWITCHING SYSTEM AND LINE SWITCHING UNIT OF DYNAMIC BAND VARIATION UNIT

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a communication system comprising data terminal devices where the data communication quantity is varied according to time, and more specifically, to a dynamic band variation unit and a switching method of a data communication quantity in a dynamic band variation unit used in the above communication system allocating the data from the data terminal device to a plurality of lines for communication of the data according to the data communication quantity of the lines.

2. Description of the Prior Art

Heretofore, as a dynamic band variation communication method connecting a dynamic band variation unit storing a data terminal device to another dynamic band variation unit storing a data terminal unit through multiple lines, there is known a communication method wherein during communication of data from one data terminal to an opposing data terminal through one communication line, another communication line is connected, and the data to be transmitted is allocated to the multiple lines so that the transfer speed of the data is increased. In this case, a clock provided to the data terminal device is increased,

and the data to be transmitted is temporarily stored in the dynamic band variation unit, so as to absorb the line delay generated between the plurality of lines. Then, the stored data is transmitted to the opposing data terminal device, thereby realizing a dynamic band variation communication utilizing a plurality of lines.

When the number of communication lines being used is decreased by disconnecting a line while communicating data through a plurality of lines in the prior art dynamic band variation communication method, either the data communicated through the disconnected line is cancelled, or the clock provided to the data terminal device from the dynamic band variation unit is reduced according to the band being reduced when disconnecting a line, and the data stored to the unit is cancelled.

SUMMARY OF THE INVENTION

However, according to the conventional method, there was a problem that the data to be transmitted from the data terminal device was not guaranteed. That is, some of the data transmitted from the data terminal device were lost when reducing the number of lines being connected, or data other than the data transmitted from the data terminal device were inserted to the data from the data terminal device when increasing the number of lines to be connected.

Therefore, according to the conventional method, the data

communicated between the data terminal devices may become defective, and only the unit having a retransmission means were able to guarantee such data.

The object of the present invention is to solve such problems of the prior art. The present invention aims at providing a line switching system and a line switching unit in a communication method for transmitting data through a plurality of lines having various delay quantities which are selected according to the status of the lines, so as to prevent the data from being lost when the number of lines is increased during communication of the data.

Even further, the present invention aims at providing a line switching unit and a line switching system of a dynamic band variation unit, wherein the data storage quantity and the data output timing for each line is calculated based on the line delay time of the plurality of lines, thereby preventing any data from being lost.

In order to solve the problems, the present invention discloses a line switching system of a dynamic band variation unit having a function to connect a dynamic data terminal device to an opposing data terminal device through a plurality of trunk lines such as dedicated lines and ISDN (integrated service and digital network) lines, said line switching system including adjusting the quantity of data stored to said dynamic band variation unit according to predetermined steps when the data communication quantity of said data terminal device is varied

by the increase or decrease in the number of lines used as trunk lines, and when said quantity of data stored to said unit is in a predetermined relation with said data communication quantity of said trunk lines, varying the data quantity to be sent out to said trunk lines.

Moreover, the present invention discloses a line switching system of a dynamic band variation unit mentioned above, wherein said line switching system further includes adjusting said quantity of data stored to said dynamic band variation unit by varying the communication speed of the data transmitted from the dynamic data terminal device before varying the data quantity to be sent out to said trunk lines, when varying said data communication quantity of the data terminal device.

Even further, the present invention discloses a line switching system of a dynamic band variation unit mentioned above, wherein said line switching system further includes measuring the line delay time determined by the difference between a line delay time of the line communicating the data and a line delay time of a line to be added, and setting the timing for transmitting data to different lines according to the line delay time of each line respectively, when increasing the number of lines.

Moreover, the present invention discloses a line switching system of a dynamic band variation unit mentioned above, wherein said line switching system further includes transmitting data to said additional line at the point of time where the quantity

of stored data equals the product of the line delay time and the data communication speed of the lines excluding a line having the largest line delay time, when increasing the number of lines.

The present invention discloses a line switching system of a dynamic band variation unit mentioned above, wherein said line switching system further includes decreasing a line at the point of time where no more quantity of data is stored, when decreasing the number of lines.

The present invention further discloses a line switching unit comprising a means for controlling the switching of a plurality of lines, a means for measuring a line delay time of said plurality of lines, a means for storing data transmitted from a data terminal device to said unit, a means for allocating said data from said data terminal device to said plurality of lines, and a means for separately controlling a clock for receiving data from said data terminal device and a clock for transmitting data to said data terminal device, wherein said line delay time of said plurality of lines is measured and the data corresponding to said line delay time is stored to said unit, said data being transferred to an opposing data terminal device in line units by a timing determined for each of said plurality of lines, so as to guarantee the data being communicated.

Moreover, the present invention discloses a line switching unit mentioned above, wherein said clock for transmitting the

data to said data terminal device is controlled to correspond to the line speed when receiving data from said line, so as to guarantee said data being communicated to said data terminal device.

According to the above mentioned invention, by allocating the data to a plurality of lines having various line delay time when communicating data from the data terminal device, the data transmitted from the data terminal device may be guaranteed while increasing or decreasing the data communication speed by connecting or disconnecting lines.

BRIEF DESCRIPTION OF DRAWINGS

FIG. 1 is an explanatory view showing the composition of the dynamic band variation communication system to which the present invention is applied;

FIG. 2 is a block diagram showing the composition of the dynamic band variation unit to which the line switching system according to the present invention is applied;

FIG. 3 is a process flowchart explaining the control of the dynamic band variation unit transmitting the data;

FIG. 4 is an explanatory view of the data transfer process of the dynamic band variation unit transmitting the data;

FIG. 5 is an explanatory view showing the state of the data transferred between the dynamic band variation units;

FIG. 6 is a process flowchart explaining the control of the dynamic band variation unit receiving the data; and

FIG. 7 is an explanatory view of the example of a data transfer process by the dynamic band variation unit receiving the data.

PREFERRED EMBODIMENT OF THE INVENTION

The embodiment of the present invention will now be explained in detail with reference to the accompanied drawings.

FIG. 1 is used to explain an example of the composition of the dynamic band variation communication system utilizing the dynamic band variation unit to which the present invention is applied.

The dynamic band variation communication method is composed of a dynamic band variation unit 10A working as a line switching unit (switching system) storing a data terminal device (DTE) 30A, and a dynamic band variation unit 10B working as a line switching unit (switching system) storing a data terminal device (DTE) 30B, which are connected by a plurality of trunk lines, such as a dedicated line 21, and line switching circuits 22, 23, 24 and the like.

In the present embodiment, the plurality of trunk lines are explained to be comprising a dedicated line 21 and line switching circuits 22 through 24, but the types or numbers of lines used as the trunk lines are not limited to such in performing the present invention.

The detailed composition of the dynamic band variation unit 10 will be explained with reference to FIG. 2.

The dynamic band variation unit 10 comprises a DTE buffer 11, a dedicated line buffer 12, a circuit line buffer 13, a delay quantity measuring means 14, a data allocation means 15, a switching circuit 16, a line control means 17, and a clock means 18.

The DTE buffer 11 operates by a clock from the clock means 18, and temporarily stores the transmitted data from the data terminal device 10.

The dedicated line buffer 12 is a buffer for temporarily storing the data to be sent out to a dedicated line 21, and has a size corresponding to the communication capacity of the dedicated line.

The circuit line buffer 13 is a buffer for temporarily storing the data to be sent out to a switching circuit line 22, and has a size corresponding to the communication capacity of the switching circuit line.

The delay quantity measuring means 14 is a means for measuring the difference between the line delay time of the dedicated line 21 and the line delay time of the switching circuit 22. The cells sent out by the same timing to each of the lines is received by the dynamic band variation unit on the other end, and the time difference in receiving the two cells is detected so as to determine the line delay quantity.

In the present specification, the difference in the line delay time of the above two lines is called the line delay quantity.

The data allocation means 15 allocates the data read out from the DTE buffer 11 to the dedicated line buffer 12 and the circuit line buffer 13.

The allocation of the data to the dedicated line buffer 12 and the circuit line buffer 13 is performed in proportion to the communication speed of each line.

Further, the starting of the data allocation is determined based on the above-mentioned line delay quantity. When the data corresponding to the line delay quantity is stored to the DTE buffer, the allocation is started.

The allocation of the data is performed as follows. The portion of the data stored in the DTE buffer 11, which had been stored thereto priorly at a time corresponding to the time of the line delay quantity, is allocated to the line buffer having a larger line delay quantity. The portion of the data stored in the DTE buffer 11, which had been stored thereto subsequently after a period of time corresponding to the time of the line delay quantity to said data allocated to the line buffer having a large line delay quantity, is allocated to the line buffer having a small line delay quantity.

The switching circuit 16 works as an electronic switching system, and connects the data stored to an input port to a predetermined line through trunks (TRK) 161, 162 and so on.

The line control means 17 controls the connection of calls or connects the switching circuit.

The clock means 18 generates clocks such as a data

transmission clock for DTE 10, a clock for the DTE buffer, a clock for the dedicated line buffer, or a clock for the circuit buffer.

When a data is transmitted through a plurality of lines, the DTE is operated by the clock having a speed corresponding to the sum of the communication speed of the plurality of lines, and the writing of the data to the DTE buffer 11 is also performed by a clock having the same speed.

FIGS. 1 through 5 are used to explain the flow of data and the process flow when the data is received from the data terminal device 30A and transmitted to the trunk line direction when the line is connected.

FIG. 3 shows the data transmission control flow in the dynamic band variation unit 10A on the data transmission side. FIG. 4 shows the flow of data in the dynamic band variation unit 10A, and FIG. 5 shows the flow of data between the dynamic band variation unit 10A on the transmitting side and the dynamic band variation unit 10B on the receiving side.

In the present explanation, the dedicated line 21 has a communication speed of 128 Kbps, and the line switching circuit 22 (hereinafter called the circuit line 22) has a communication speed of 64 Kbps. An example is explained where the circuit line 22 is additionally used when communicating data through the dedicated line 21 by a communication speed of 128 Kbps, thereby transmitting data by a communication speed of 192 Kbps in total.

For means of explanation, it is assumed that the dedicated line 21 has a line delay time of one unit time (for example, 18 msec), and the circuit line 22 has a line delay time of four unit time. Thereby, the line delay quantity equals three unit time, and the data that traveled through the circuit line 22 will be delayed for three unit time compared to the data that traveled through the dedicated line 21.

When the data is communicated through the dedicated line 21 (FIG. 3, S11), the data is sent out from the DTE 30A from a unit time T1 to a unit time T6 by a communication speed of 128 Kbps. Per one unit time, 288 bytes of data is stored to the DTE buffer 11. In FIGS. 4 and 5, 144 bytes of data is shown as one unit.

In unit time T1, 288 bytes of data 1-1, 1-2 is stored to the DTE buffer 11, and the data is then transferred to the dedicated line buffer 12, and transmitted through the dedicated line 21.

In unit time T2, the data 2-1, 2-2 is stored to the DTE buffer 11, and the data is then transferred to the dedicated line buffer 12, and transmitted through the dedicated line 21.

Similarly during unit time T3 through unit time T6, the data 3-1 through 6-2 is transmitted to the dedicated line 21 by units of 288 bytes.

When a condition to increase the data communication quantity from the data terminal device 30A, such as increase of traffic and the like, is fulfilled at unit time T7 while data

is communicated between the data terminal device 30A and the data terminal device 30B through the dedicated line 21, a call is generated from the dynamic band variation unit 10A through the circuit line 22, so as to form a connection with the opposing dynamic band variation unit 10B (FIG. 3, S12).

When the connection in the circuit line 22 is completed, the line delay quantity of the dedicated line 21 and the circuit line 22 is measured (FIG. 3, S13).

The measurement of the line delay quantity is performed for example as follows. The delay quantity measuring means 14 outputs the same data at the same timing to the opposing dynamic band variation unit 10B through both the dedicated line 21 and the circuit line 22. Based on the line delay time of the data received by the dynamic band variation unit 10B through the dedicated line 21 and the data received through the circuit line 22, the line delay quantity data, which is the difference between the two line delay times measured above, is determined. This line delay quantity data is notified to the dynamic band variation unit 10A on the transmission side.

In the example shown in FIGS. 4 and 5, the time needed to measure the line delay quantity data and the time needed to notify the data to the dynamic band variation unit 10A on the transmission side is assumed to be 0, so as to simplify the explanation.

Simultaneously as the measurement of the line delay quantity data, the clock means 18 sets the data transfer clock

speed, from the data terminal device 30A to the DTE buffer 11A, to the sum speed (for example, 192 Kbps) of the transfer clock speed of the dedicated line 21 (for example, 128 Kbps) and the transfer clock speed of the circuit line 22 (for example, 64 Kbps) (FIG. 3, S14).

At unit time T7, the data 7-1, 7-2, 7-3 having a total of 432 bytes transmitted from the data terminal device 30A by a communication speed of 192 Kbps is stored to the DTE buffer 11. The data 7-1, 7-2 of 288 bytes written at unit time T7 is transferred to the dedicated line buffer 12 and sent out to the dedicated line 21.

The data 7-3 of 144 bytes will remain in the DTE buffer 11 (FIG. 3, S15).

At unit time T8, the data 8-1, 8-2, 8-3 transmitted from the data terminal device 30A is stored to the DTE buffer 11. The data 7-3 written at unit time T7 and the data 8-1 written at unit time T8 is transferred to the dedicated line buffer 12 and sent out to the dedicated line 21.

The data 8-2, 8-3 of 288 bytes remains in the DTE buffer 11.

Similarly, at unit time T9, the data 9-1, 9-2, 9-3 from the data terminal device 30A is stored to the DTE buffer. The remaining 288-byte-data 8-2, 8-3 written at unit time T8 is transferred to the dedicated line buffer 12 and outputted to the dedicated line 21.

The data 9-1, 9-2, 9-3 of 432 bytes remains in the DTE buffer

11 (FIG. 3, S15).

As explained, 144 bytes of data per one unit time is stored to the DTE buffer 11.

The above-mentioned process is repeatedly performed, and at unit time T12, the 432 bytes of data 12-1, 12-2, 12-3 from the data terminal device 30A is stored to the DTE buffer. The 288 bytes of data 10-2, 10-3 written at unit time T10 is transferred to the dedicated line buffer 12 and outputted to the dedicated line 21.

A total of 864 bytes of data comprising the data 11-1, 11-2, 11-3 written at unit time T11 and the data 12-1, 12-2, 12-3 written at unit time T12 remains in the DTE buffer 11.

At unit time T13, it is detected that data corresponding to the line delay quantity is stored in the DTE buffer 11 (FIG. 3, S16). The 432 bytes of data 13-1, 13-2, 13-3 from the data terminal device 30A is stored to the DTE buffer 11, and the 288 bytes of data 11-1, 11-2 written at unit time T11 is transferred to the dedicated line buffer 12, and outputted to the dedicated line 21. At the same time, the 144 bytes of data 13-3 written at unit time T13 is transferred to the circuit line buffer 13, and transmitted to the circuit line 22 (FIG. 3, S17).

The 144 bytes of data 11-3 written at unit time T11, the 432 bytes of data 12-1, 12-2, 12-3 written at unit time T12, and the 288 bytes of data 13-1, 13-2 written at unit time T13, which totals to 864 bytes of data, remains in the DTE buffer 11.

At unit time T14, the data 14-1, 14-2, 14-3 from the data terminal device 30A is stored to the DTE buffer 11. The 144 bytes of data 11-3 written at unit time T11 and the 144 bytes of data 12-1 written at unit time T12, which totals to 288 bytes of data, is transferred to the dedicated line buffer 12 and outputted to the dedicated line 21. The data 14-3 written at unit time T14 is transferred to the circuit line buffer 13 and outputted to the circuit line 22.

The data 12-2, 12-3 written at unit time T12, the data 13-1, 13-2 written at unit time T13 and the data 14-1, 14-2 written at unit time T14, which totals to 864 bytes of data, remains in the DTE buffer 11.

At unit time T15, the data 15-1, 15-2, 15-3 from the data terminal device 30A is stored to the DTE buffer 11. The data 12-2, 12-3 written at unit time T12 is transferred to the dedicated line buffer 12 for output to the dedicated line 21. At the same time, the data 15-3 written at unit time T15 is transferred to the circuit line buffer 13 and outputted to the circuit line 22.

The data 13-1, 13-2 written at unit time T13, the data 14-1, 14-2 written at unit time T14, and the data 15-1, 15-2 written at unit time T15, which totals to 864 bytes of data, remains in the DTE buffer 11.

At unit time T16, the data 16-1, 16-2, 16-3 from the data terminal device 30A is stored to the DTE buffer 11. The data 13-1, 13-2 written at unit time T13 is transferred to the

dedicated line buffer 12 for output to the dedicated line 21. At the same time, the data 16-3 written at unit time T16 is transferred to the circuit line buffer 13 and outputted to the circuit line 22.

The data 14-1, 14-2 written at unit time T14, the data 15-1, 15-2 written at unit time T15, and the data 16-1 and 16-2 written at unit time T16, which totals to 864 bytes of data, remains in the DTE buffer 11.

Similarly, the amount of data corresponding to the line delay quantity, in other words, the amount of data that may be transferred through a communication path having a smaller line delay time in three unit time, may be stored to the DTE buffer 11, and the data inputted during the present unit time is outputted to the circuit line 22 having a delay quantity corresponding to three unit time. At the same time, the data written three unit time earlier is outputted to the dedicated line 21, and the data is communicated by a total speed of 192 Kbps.

The amount of data stored to the DTE buffer 11, in other words, the data quantity Db corresponding to the line delay quantity may be shown by formula (1), in which the communication speed of the line having a small line delay time is shown as Sd.

$$Db = Td \times Sd \cdots (1)$$

Moreover, the time needed after adding a new communication path during communication before transferring the data to the

additional transmission path, that is, time Ts needed to store the amount of data Db corresponding to the line delay time, may be shown by formula (2), wherein the communication speed of the line having a small line delay time is shown as Sd, and the total communication speed of the line is shown as St.

$$Ts = Db/St-Sd \cdots (2)$$

Even further, when adding another line while communicating through a plurality of lines, the amount of data stored in the DTE buffer 11 or amount of data Db corresponding to the line delay quantity may be shown by formula (3), wherein the line delay quantity shown by the difference between the line delay time of the line having the smallest line delay time and the line delay time of the line having the largest line delay time is shown as Td, and the total speed of communication by the plurality of lines other than the newly added line is shown as Ss.

$$Db = Td \times Ss \cdots (3)$$

With reference to FIGS. 5 through 7, the process flow for transferring the data received by the dynamic band variation unit 10B on the receiving side to the data terminal device 30B when an additional line is added during communication shown in FIGS. 4 and 5 is explained.

In the present embodiment, the line delay time of the dedicated line 21 is assumed to be one unit time. Therefore, the data transmitted to the dedicated line 21 at unit time T1 will reach the receiving dynamic band variation unit 10B at unit

time T2. However, in order to match the unit time of the transmitting unit and that of the receiving unit, the unit time at which the first data arrives to the receiver is explained as T1'.

At unit time T1', the 288 bytes of data 1-1, 1-2 sent out at unit time T1 through the dedicated line 21 is received by the dedicated line buffer 12B.

The data 1-1, 1-2 will be transferred to the DTE buffer 11B, and further transferred to the data terminal device 30B by a communication speed of 128 Kbps (FIG. 6, S21).

Similarly, the data 2-1 through 7-2 sent out through the dedicated line 21 during unit time T2 through T7 is received at unit time T2' through T7'by the dedicated line buffer 12B in units of 288 bytes.

The data 2-1 through 7-2 is transferred to the DTE buffer 11B, and further transferred to the data terminal device 30B by a communication speed of 128 Kbps.

At unit time T8', the 144-byte-data 7-3 sent out at unit time T7 and the 144-byte-data 8-1 sent out at unit time T8 through the dedicated line 21 is received at the dedicated line buffer 12B.

The data 7-3, 8-1 is transferred to the DTE buffer 11B, and further transferred to the data terminal device 30B by a communication speed of 128 Kbps.

At unit time T9', the 288 bytes of data 8-2, 8-3 sent out at unit time T8 through the dedicated line 21 is received at

the dedicated line buffer 12B.

The data 8-2 and 8-3 is transferred to the DTE buffer 11B, and further transferred to the data terminal device 30B by a communication speed of 128 Kbps.

Similarly, at unit time T10'-T15', the 288 bytes of data 9-1, 9-2 transmitted at unit time T9 to the 288 bytes of data 12-2, 12-3 transmitted at unit time T15 through the dedicated line 21 is received at the dedicated line buffer 12B.

The data 9-1 through 12-3 is transferred to the DTE buffer 11B by units of 288 bytes, and further transferred to the data terminal device 30B by a communication speed of 128 Kbps.

During this time, it is observed whether data is received from the circuit line 22 (FIG. 6, S22).

When data from the circuit line 22 is received at unit time T16' (FIG. 6, S22), the clock generation means 18B sets a 192 Kbps data reception clock to the data terminal device 30B (FIG. 6, S23). The receiving dynamic band variation unit 10B receives the 288-byte-data 13-1, 13-2 sent out at unit time T16 through the dedicated line 21 by the dedicated line buffer 12B, and at the same time, receives the 144-byte-data 13-3 sent out at unit time T13 through the circuit line 22 by the circuit line buffer 13B.

The 288 bytes of data 13-1, 13-2 received by the dedicated line buffer 12B and the 144 bytes of data 13-3 received by the circuit line buffer 13B is transferred to the DTE buffer 11B respectively, and further transferred to the data terminal

device 30B by a communication speed of 192 Kbps (FIG. 6, S24).

After that, a data of 432 bytes in total arriving at the same timing through both the dedicated line 21 and the circuit line 22 is transferred to the DTE 30B through the DTE buffer 11B by a communication speed of 192 Kbps.

Thereafter, 432 bytes of data in total is received by the dedicated line buffer 12B and the circuit line buffer 13B, which will be transferred to the DTE30B through the DTE buffer 11B by a communication speed of 192 Kbps.

When communicating according to the above-mentioned steps, it may be possible to transfer the data transmitted from the data terminal device 30A to the data terminal device 30B without any data loss.

The steps for cutting the circuit line 22 and reducing the communication quantity of the data will now be explained.

When condition such as reduction in traffic and the like is fulfilled to reduce the data communication quantity from the data terminal device 30A, the dynamic band variation unit 10A sets the transmission clock (192 Kbps) of the data transmitted from the data terminal device 30A to the communication speed of the dedicated line, which is 128 Kbps. When transmission of the data through the dedicated line 21 and the circuit line 22 is continued under such condition, the amount of data stored to the DTE buffer 11A will be reduced in proportion to time. When the stored data is gone, the transmission of the data to the circuit line 22 is stopped, so as to return to the state

where communication is performed only by the dedicated line 21.

On the other hand, when the receiving dynamic band variation unit 10B detects that no more data is transmitted through the circuit line 22 while receiving data from both the dedicated line 21 and the circuit line 22 as shown in FIG. 7, the transfer of data from the circuit line buffer 13B to the DTE buffer 13B is terminated, and the data reception clock to the data terminal device 30B is set to the communication speed of the dedicated line 21 (128 Kbps).

This process enables to recover the initial communication state where only the dedicated line 21 is used for the communication of data.

As mentioned above, the present invention provides a data communication system using a dynamic band variation unit where the lines used for communication may be increased or decreased while guaranteeing the data transmitted between two data terminal devices, and the data from one data terminal device may be allocated to a plurality of lines for communication to the other data terminal device.

We claim:

1. A line switching system of a dynamic band variation unit having a function to connect a dynamic data terminal device to an opposing data terminal device through a plurality of trunk lines such as dedicated lines and ISDN lines, said line switching system including:

adjusting the quantity of data stored to said dynamic band variation unit according to predetermined steps when varying the data communication quantity of said data terminal device by increasing or decreasing the number of lines used as trunk lines, and when said quantity of data stored to said unit comes to be in a predetermined relation with said data communication quantity of said trunk lines, varying the quantity of data to be sent out to said trunk lines, thereby preventing loss of said data.

2. A line switching system of a dynamic band variation unit according to claim 1, wherein said line switching system further includes adjusting said quantity of data stored to said dynamic band variation unit by varying the communication speed for transmitting data from the dynamic data terminal device, before varying the quantity of data to be sent out to said trunk lines, when varying said data communication quantity of said data terminal device.

3. A line switching system of a dynamic band variation unit

according to claim 2, wherein said line switching system further includes measuring the line delay time determined by the difference between a line delay time of the line communicating the data and a line delay time of a line to be added, and setting the timing for sending out data to different lines respectively according to the line delay time of each line, when increasing the number of lines.

4. A line switching system of a dynamic band variation unit according to claim 3, wherein said line switching system further includes sending out data to said additional line at the point of time where the quantity of stored data equals the product of the line delay time and the data communication speed of the lines excluding a line having the largest line delay time, when increasing the number of lines.

5. A line switching system of a dynamic band variation unit according to claim 2, wherein said line switching system further includes decreasing the number of lines at the point of time where no more quantity of data is stored.

6. A line switching unit comprising:

a means for controlling the switching of a plurality of lines;

a means for measuring a line delay time of said plurality of lines;

a means for storing data transmitted from a data terminal device to said unit;

a means for allocating said data from said data terminal device to said plurality of lines; and

a means for separately controlling a clock for receiving data from said data terminal device and a clock for transmitting data to said data terminal device;

wherein said line delay time of said plurality of lines are measured and the data corresponding to said line delay time is stored to said unit, said data being transferred to an opposing data terminal device in units through said plurality of lines by a timing determined for each of said plurality of lines, thereby guaranteeing the data being communicated.

7. A line switching unit according to claim 6, wherein said clock for transmitting the data to said data terminal device is controlled to correspond to the line speed when receiving data from said line, thereby guaranteeing said data being communicated to said data terminal device.

ABSTRACT

A line switching system of a dynamic band variation unit 10 having a function for connecting a dynamic data terminal device 30A to an opposing data terminal device 30B through a plurality of trunk lines such as a dedicated line 21 or ISDN lines 22 through 24, wherein the quantity of data to be sent out to a trunk line is varied after the quantity of data to be stored to the dynamic band variation unit is adjusted by varying the communication speed of the data transmitted from the dynamic data terminal unit, when varying the data communication quantity of the data terminal device by increasing or decreasing the number of trunk lines.

Fig. 1

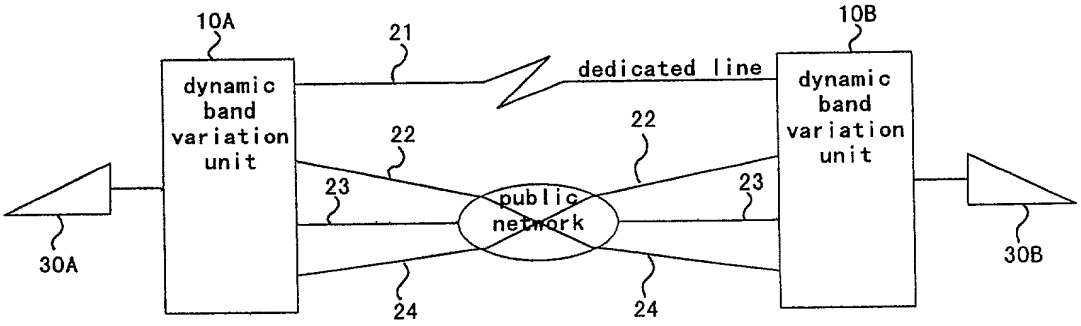

10A
21
dedicated line
10B
dynamic band variation unit
dynamic band variation unit
22
22
23
23
public network
30A
30B
24
24

Fig. 2

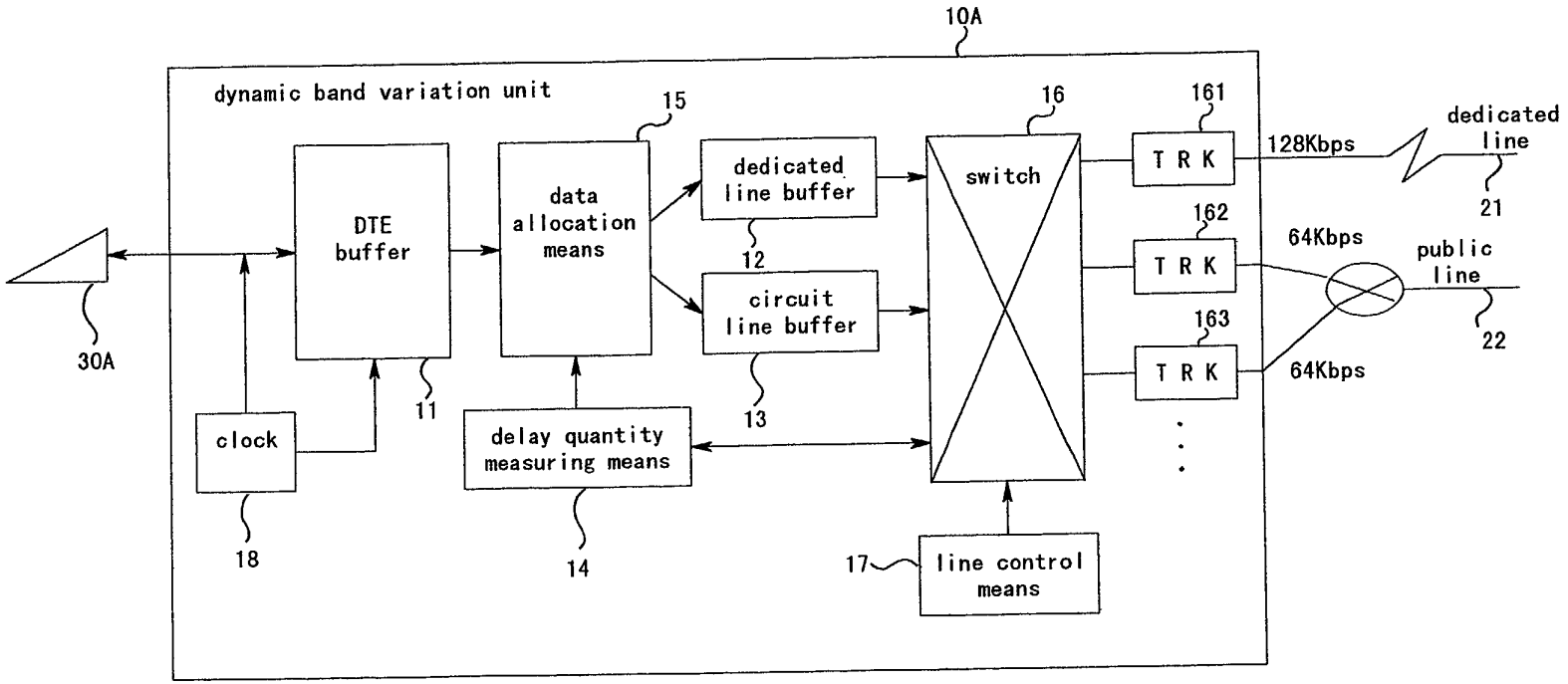

10A
dynamic band variation unit
15
16
161
dedicated line
128Kbps
DTE buffer
data allocation means
dedicated line buffer
switch
T R K
21
12
162
64Kbps
public line
circuit line buffer
T R K
30A
11
163
22
T R K
64Kbps
clock
delay quantity measuring means
13
18
14
17
line control means

Fig. 3

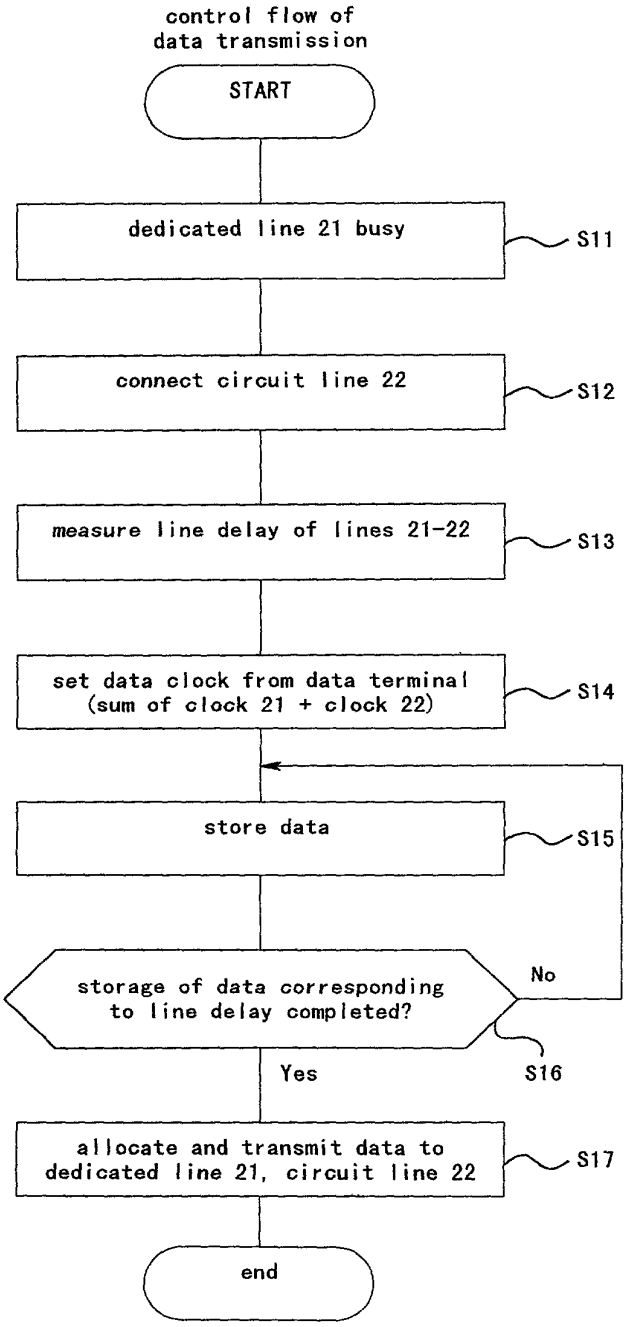

control flow of
data transmission
START
dedicated line 21 busy
S11
connect circuit line 22
S12
measure line delay of lines 21-22
S13
set data clock from data terminal
(sum of clock 21 + clock 22)
S14
store data
S15
storage of data corresponding
to line delay completed?
No
Yes
S16
allocate and transmit data to
dedicated line 21, circuit line 22
S17
end

Fig. 4

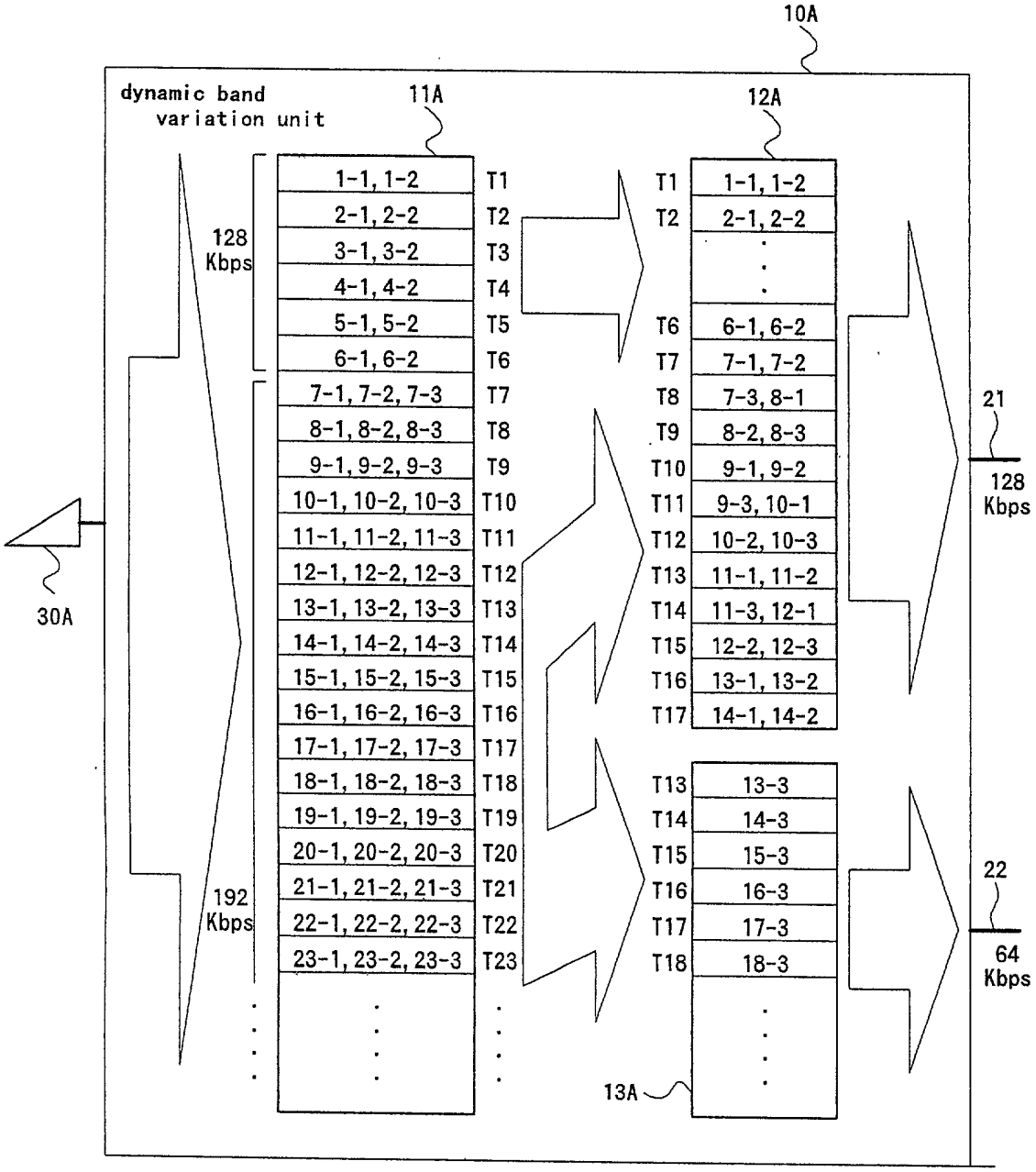

10A
dynamic band variation unit
11A
12A
128 Kbps
192 Kbps
30A
21
128 Kbps
22
64 Kbps
13A
1-1, 1-2 T1
2-1, 2-2 T2
3-1, 3-2 T3
4-1, 4-2 T4
5-1, 5-2 T5
6-1, 6-2 T6
7-1, 7-2, 7-3 T7
8-1, 8-2, 8-3 T8
9-1, 9-2, 9-3 T9
10-1, 10-2, 10-3 T10
11-1, 11-2, 11-3 T11
12-1, 12-2, 12-3 T12
13-1, 13-2, 13-3 T13
14-1, 14-2, 14-3 T14
15-1, 15-2, 15-3 T15
16-1, 16-2, 16-3 T16
17-1, 17-2, 17-3 T17
18-1, 18-2, 18-3 T18
19-1, 19-2, 19-3 T19
20-1, 20-2, 20-3 T20
21-1, 21-2, 21-3 T21
22-1, 22-2, 22-3 T22
23-1, 23-2, 23-3 T23
T1 1-1, 1-2
T2 2-1, 2-2
T6 6-1, 6-2
T7 7-1, 7-2
T8 7-3, 8-1
T9 8-2, 8-3
T10 9-1, 9-2
T11 9-3, 10-1
T12 10-2, 10-3
T13 11-1, 11-2
T14 11-3, 12-1
T15 12-2, 12-3
T16 13-1, 13-2
T17 14-1, 14-2
T13 13-3
T14 14-3
T15 15-3
T16 16-3
T17 17-3
T18 18-3

Fig. 5

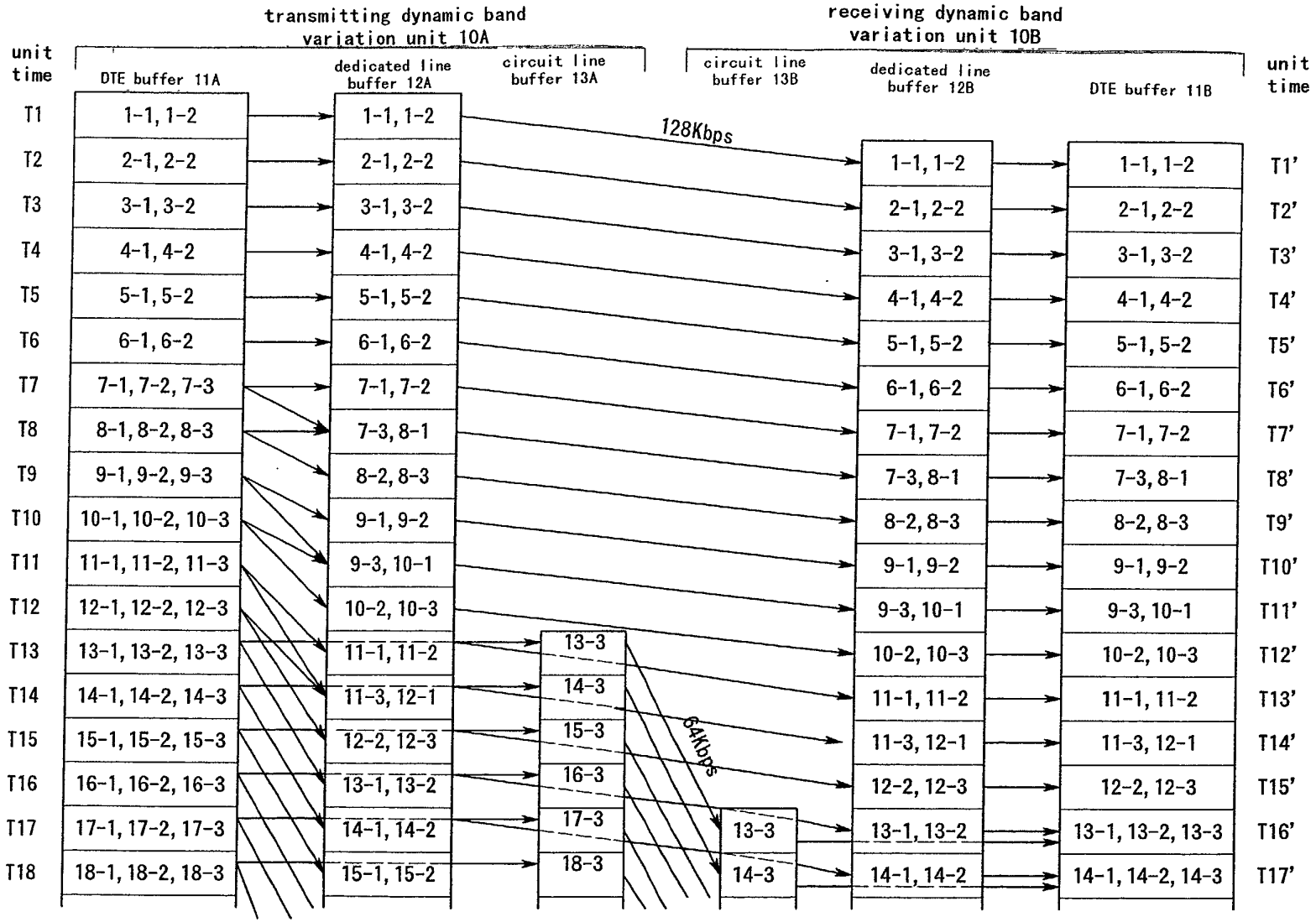

transmitting dynamic band variation unit 10A
receiving dynamic band variation unit 10B
unit time
DTE buffer 11A
dedicated line buffer 12A
circuit line buffer 13A
circuit line buffer 13B
dedicated line buffer 12B
DTE buffer 11B
128Kbps
64Kbps
T1 1-1, 1-2
T2 2-1, 2-2
T3 3-1, 3-2
T4 4-1, 4-2
T5 5-1, 5-2
T6 6-1, 6-2
T7 7-1, 7-2, 7-3
T8 8-1, 8-2, 8-3
T9 9-1, 9-2, 9-3
T10 10-1, 10-2, 10-3
T11 11-1, 11-2, 11-3
T12 12-1, 12-2, 12-3
T13 13-1, 13-2, 13-3
T14 14-1, 14-2, 14-3
T15 15-1, 15-2, 15-3
T16 16-1, 16-2, 16-3
T17 17-1, 17-2, 17-3
T18 18-1, 18-2, 18-3
1-1, 1-2
2-1, 2-2
3-1, 3-2
4-1, 4-2
5-1, 5-2
6-1, 6-2
7-1, 7-2
7-3, 8-1
8-2, 8-3
9-1, 9-2
9-3, 10-1
10-2, 10-3
11-1, 11-2
11-3, 12-1
12-2, 12-3
13-1, 13-2
14-1, 14-2
15-1, 15-2
13-3
14-3
15-3
16-3
17-3
18-3
13-3
14-3
1-1, 1-2
2-1, 2-2
3-1, 3-2
4-1, 4-2
5-1, 5-2
6-1, 6-2
7-1, 7-2
7-3, 8-1
8-2, 8-3
9-1, 9-2
9-3, 10-1
10-2, 10-3
11-1, 11-2
11-3, 12-1
12-2, 12-3
13-1, 13-2
14-1, 14-2
1-1, 1-2
2-1, 2-2
3-1, 3-2
4-1, 4-2
5-1, 5-2
6-1, 6-2
7-1, 7-2
7-3, 8-1
8-2, 8-3
9-1, 9-2
9-3, 10-1
10-2, 10-3
11-1, 11-2
11-3, 12-1
12-2, 12-3
13-1, 13-2, 13-3
14-1, 14-2, 14-3
unit time
T1' T2' T3' T4' T5' T6' T7' T8' T9' T10' T11' T12' T13' T14' T15' T16' T17'

Fig. 6

control flow of
data reception

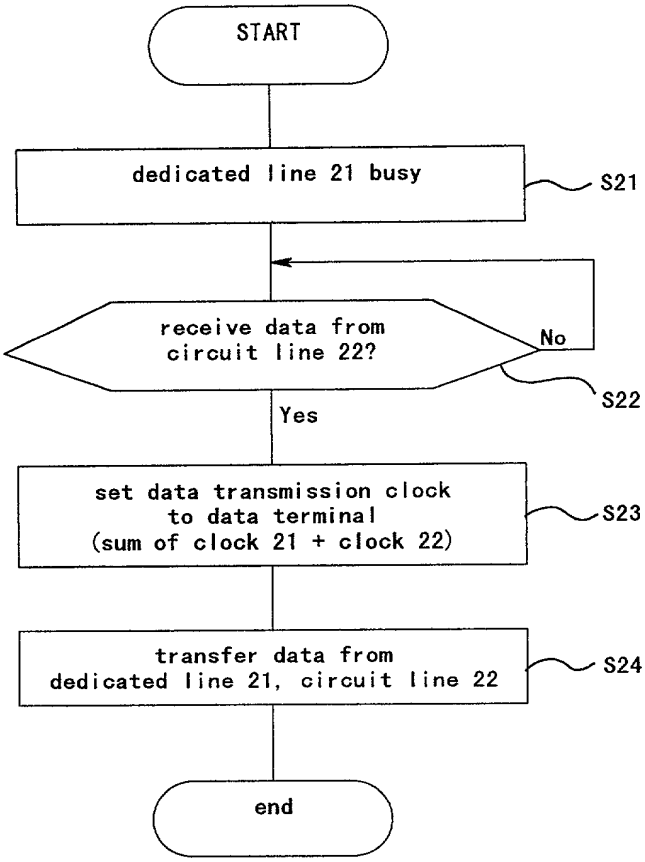
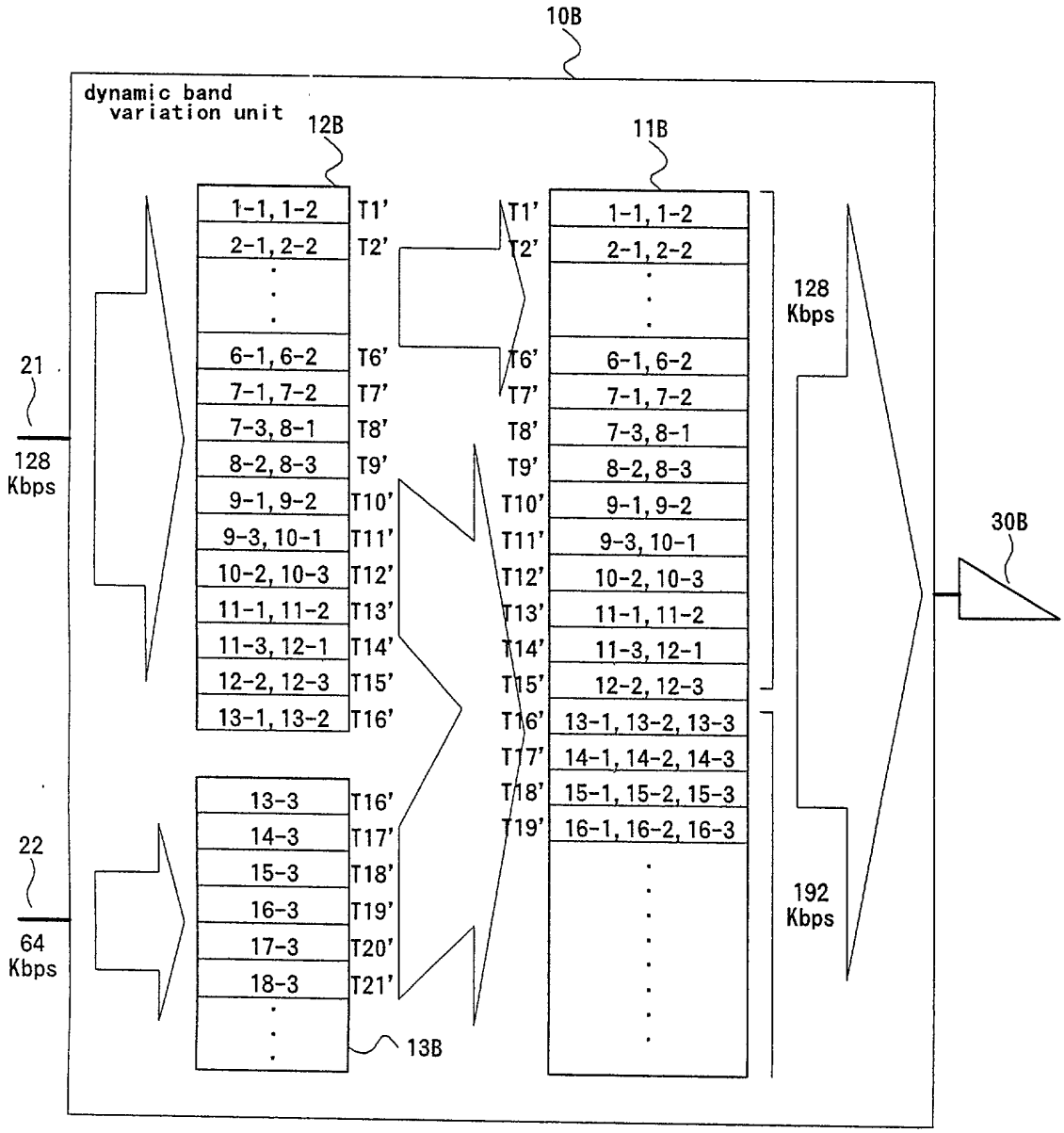


Fig. 7


10B
dynamic band variation unit
12B
11B
1-1, 1-2 T1'
2-1, 2-2 T2'
6-1, 6-2 T6'
7-1, 7-2 T7'
7-3, 8-1 T8'
8-2, 8-3 T9'
9-1, 9-2 T10'
9-3, 10-1 T11'
10-2, 10-3 T12'
11-1, 11-2 T13'
11-3, 12-1 T14'
12-2, 12-3 T15'
13-1, 13-2 T16'
13-3 T16'
14-3 T17'
15-3 T18'
16-3 T19'
17-3 T20'
18-3 T21'
13B
T1' 1-1, 1-2
T2' 2-1, 2-2
T6' 6-1, 6-2
T7' 7-1, 7-2
T8' 7-3, 8-1
T9' 8-2, 8-3
T10' 9-1, 9-2
T11' 9-3, 10-1
T12' 10-2, 10-3
T13' 11-1, 11-2
T14' 11-3, 12-1
T15' 12-2, 12-3
T16' 13-1, 13-2, 13-3
T17' 14-1, 14-2, 14-3
T18' 15-1, 15-2, 15-3
T19' 16-1, 16-2, 16-3
128 Kbps
192 Kbps
21
128 Kbps
22
64 Kbps
30B

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor, I/we hereby declare that:

My/Our residence, post office address and citizenship are as stated below next to my/our name, I/we believe that I/we are the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

LINE SWITCHING SYSTEM AND LINE SWITCHING UNIT OF DYNAMIC BAND VARIATION UNIT,

the specification of which (check one)

☐ is attached hereto.

☐ was filed on _____
as Application Serial No. _____
and was amended on _____ .
(if applicable)

I/We hereby state that I/we have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I/We acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a).

I/We hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Claimed	
H10-128973 (Number)	Japan (Country)	12/05/1998 (Day/Month/Year Filed)	[X] Yes	[ ] No
(Number)	(Country)	(Day/Month/Year Filed)	[ ] Yes	[ ] No
(Number)	(Country)	(Day/Month/Year Filed)	[ ] Yes	[ ] No
(Number)	(Country)	(Day/Month/Year Filed)	[ ] Yes	[ ] No
(Number)	(Country)	(Day/Month/Year Filed)	[ ] Yes	[ ] No
(Number)	(Country)	(Day/Month/Year Filed)	[ ] Yes	[ ] No

I/We hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I/we acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application and the national or PCT internatinal filing date of this application:

(Application Serial No.)	(Filing Date)	(Status: patented, pending, abandoned)
(Application Serial No.)	(Filing Date)	(Status: patented, pending, abandoned)
(Application Serial No.)	(Filing Date)	(Status: patented, pending, abandoned)
(Application Serial No.)	(Filing Date)	(Status: patented, pending, abandoned)

(Continued on Page 2)

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further, that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United State Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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